1. General Information

1a. Submitted by the College of: ENGINEERING

Date Submitted: 9/29/2015

1b. Department/Division: Electrical and Computer Engineering

1c. Contact Person

Name: James Lumpp

Email: jel@uky.edu

Phone: 7-3895

Responsible Faculty ID (if different from Contact)

Name:

Email:

Phone:

1d. Requested Effective Date: Semester following approval

1e. Should this course be a UK Core Course? No

2. Designation and Description of Proposed Course

2a. Will this course also be offered through Distance Learning?: No

2b. Prefix and Number: EE 282

2c. Full Title: Digital Logic Design

2d. Transcript Title:

2e. Cross-listing: CpE 282

2f. Meeting Patterns

LECTURE: 3

LABORATORY: 3

2g. Grading System: Letter (A, B, C, etc.)

2h. Number of credit hours: 4

2i. Is this course repeatable for additional credit? No

If Yes: Maximum number of credit hours:

If Yes: Will this course allow multiple registrations during the same semester?

2j. Course Description for Bulletin: Boolean algebra; number systems; combinational logic circuits; synchronous sequential circuits; asynchronous sequential circuits; design problems using digital logic. Laboratory experiments reinforce the course content. Lecture, three hours; laboratory, one three-hour session.

2k. Prerequisites, if any: EGR 102 or equivalent programming course.

2l. Supplementary Teaching Component:

3. Will this course taught off campus?   No

   If YES, enter the off campus address:

4. Frequency of Course Offering: Spring,

   Will the course be offered every year?:   Yes

   If No, explain:

5. Are facilities and personnel necessary for the proposed new course available?:   Yes

   If No, explain:

6. What enrollment (per section per semester) may reasonably be expected?:   175

7. Anticipated Student Demand

   Will this course serve students primarily within the degree program?:   Yes

   Will it be of interest to a significant number of students outside the degree pgm?:   Yes

   If Yes, explain: Required by BS Computer Engineering and BS Electrical Engineering degrees.

8. Check the category most applicable to this course: Traditional – Offered in Corresponding Departments at Universities Elsewhere,

   If No, explain:

9. Course Relationship to Program(s).

   a. Is this course part of a proposed new program?:   No

   If YES, name the proposed new program:

   b. Will this course be a new requirement for ANY program?:   Yes

   If YES, list affected programs: BS Computer Engineering and BS Electrical Engineering

10. Information to be Placed on Syllabus.

   a. Is the course 400G or 500?:   No

   b. The syllabus, including course description, student learning outcomes, and grading policies (and 400G-/500-level grading differentiation if applicable, from **10.a** above) are attached: Yes

Distance Learning Form

Instructor Name:

Instructor Email:

Internet/Web-based: No

Interactive Video: No

Hybrid: No

1.How does this course provide for timely and appropriate interaction between students and faculty and among students? Does the course syllabus conform to University Senate Syllabus Guidelines, specifically the Distance Learning Considerations?

2.How do you ensure that the experience for a DL student is comparable to that of a classroom-based student's experience? Aspects to explore: textbooks, course goals, assessment of student learning outcomes, etc.

3.How is the integrity of student work ensured? Please speak to aspects such as password-protected course portals, proctors for exams at interactive video sites; academic offense policy; etc.

4.Will offering this course via DL result in at least 25% or at least 50% (based on total credit hours required for completion) of a degree program being offered via any form of DL, as defined above?

If yes, which percentage, and which program(s)?

5.How are students taking the course via DL assured of equivalent access to student services, similar to that of a student taking the class in a traditional classroom setting?

6.How do course requirements ensure that students make appropriate use of learning resources?

7.Please explain specifically how access is provided to laboratories, facilities, and equipment appropriate to the course or program.

8.How are students informed of procedures for resolving technical complaints? Does the syllabus list the entities available to offer technical help with the delivery and/or receipt of the course, such as the Information Technology Customer Service Center (http://www.uky.edu/UKIT/)?

9.Will the course be delivered via services available through the Distance Learning Program (DLP) and the Academic Technology Group (ATL)?   NO

If no, explain how student enrolled in DL courses are able to use the technology employed, as well as how students will be provided with assistance in using said technology.

10.Does the syllabus contain all the required components?   NO

11.I, the instructor of record, have read and understood all of the university-level statements regarding DL.

Instructor Name:

SIGNATURE|HOLLOWAY|Lawrence E Holloway|EE 282 NEW Dept Review|20150930

SIGNATURE|BJSTOK0|Barbara J Brandenburg|EE 282 NEW College Review|20151022

SIGNATURE|JMETT2|Joanie Ett-Mims|EE 282 NEW Undergrad Council Review|20160112

EE 282
Digital Logic Design

Instructor:	Dr. Jeffery Ashley
Office Address:	453 F. Paul Anderson Tower, 0046
Email:	jeffery.ashley@uky.edu (preferred contact method)
Office Phone:	257-8042

Office hours:	M and W, 2 to 3:30 PM (or by appointment)
Lectures:	MWF1-1:50, 257 FPAT
Lab Sections 581FPAT:	
001:	M 2-5
002:	T 2-5
003:	Th 2-5

Course Description: Boolean algebra; number systems; combinational logic circuits; synchronous sequential circuits; asynchronous sequential circuits; design problems using digital logic. Laboratory experiments reinforce the course content. Lecture, three hours; laboratory, one three-hour session.

Prerequisites: EGR 102 or equivalent programming course.

Student Learning Outcomes:

Students who fulfill the requirements for this course will be able to:
Upon successful completion of EE 282 students will be able to:
1. Perform arithmetic in various number systems.
2. Apply Boolean algebra to design and minimize logic circuits.
3. Design combinational logic circuits and use computer simulation to verify correct design and operation of the circuits.
4. Design sequential logic circuits and use computer simulation to verify correct design and operation of the circuits.
5. Apply timing analysis and other techniques in the design of reliable logic circuits.

Required Materials:

Fundamentals of Digial Logic with Verilog Design, Third Edition, Stephen Brown and Zvonko Vranesic, McGraw-Hill, 2013, ISBN 978-0-07-338054-4

Lab Supplies: students are required to purchase a parts kit for this course and each student must have a breadboard, wire, and a wire stripper. The contents of the kit will be discussed in class and is listed on the course web page. You can purchase the parts from Radio Shack, on-line parts vendors, or from the IEEE Parts Store FPAT560.

Description of Course Activities and Assignments
Course Assignments
Homework, quizzes, lab and project reports will be submitted on paper and/or graded via Canvas. Midterm exams will be given in class and the final exam will be given during finals week.

Homework	04%	15 homework assignments, 20 points each
Quizzes	08%	10 quizzes, 10 points each
Design Experiments	20%	6 laboratory experiments, 50 points each
Exam 1	16%	
Exam 2	16%	
Exam 3	16%	
Final Exam	20%	

Summary Description of Course Assignments

Homework will be assigned to reinforce topics read in the book and discussed in class and assess course outcomes 1 through 5 above. Homework assignments will be collected and graded weekly. Partial credit will be based on work shown. Correct answers to problems that require substantial work may not get full credit if not enough work is present to demonstrate how the student solved the problem.
Homework assignments may be written in pen or pencil, but should be neat enough to be legible. Illegible answers will be considered incorrect. Some homework problems may be collected and graded through a web form.

Quizzes will be given approximately once every one to two weeks to reinforce material covered in the homework. The lowest quiz score will be dropped at the end of the semester. Quizzes will assess all five course outcomes. A quiz missed due to an unexcused absence will receive a zero and cannot be made up.

Three exams and a comprehensive final exam will be given to assess student's progress in the class. You will take the first exam upon completion of Chapter 4. You will take the second exam after the completion of Chapter 6 and test 3 upon completing Chapter 8. I will give you at least one week advanced notice on the exact date of these tests. The final exam will be scheduled per University Guidelines and will be taken during finals week. The final will be comprehensive.

Missed homework, quizzes and exams may be made up for excused absences per UK *Senate Rules 5.2.4.2* (discussed below).

Course Grading

Grading Scale
>   90 – 100% = A
>   80 – 89% = B
>   70 – 79% = C
>   60 – 69% = D
>   < 60% = E

Tentative Course Schedule
Q = quiz on reading and technical content
E = Exam
HW = homework problems, drawings, calculations, etc
L = Laboratory Experiment

Weeks	Topic	Text Reading	Assignments
1	Introduction - Chapter 1 Logic functions and Boolean algebra	1.1-1.6 2.1- 2.5	HW1
2	Synthesis of combinational circuits with AND, OR, NOT gates, Synthesis with NAND and NOR gates	2.6 2.7, 2.8	L2, HW2, Q1
3	Expressing logic circuits in Verilog Karnaugh Maps	2.9- 2.10 2.11-2.15	HW3, Q2
4	Unsigned numbers and arithmetic	3.1,3.2	L2, HW4, Q3
5	Signed numbers and arithmetic Fast Adders	3.3 3.4	E1, HW5
6	Arithmetic circuits in Verilog Multiplication and other number representations	3.5 3.6-3.7	L3, HW6, Q4
7	Multiplexers and Shannon's Expansion Theorem Decoders, encoders, converters, and comparators	4.1 4.2-4.5	HW7, Q5
8	Building blocks in Verilog	4.6	HW8
9	Introduction to sequential circuits; latches D, JK, and T Flip-flops	5.1- 5.3 5.4- 5.7	E2, HW9
10	Registers, shift registers, and counters Reset synchronization and more counter	5.8, 5.9 5.10, 5.11	L4, HW10, Q6
11	Sequential behavior in Verilog Timing Analysis	5.12- 5.14 5.15	HW11, Q7
12	Synchronous design with finite state machines (FSMs) FSMs in Verilog	6.1- 6.3 6.4, 6.5	L5, HW12
13	State minimization and unused states	6.6	E3, HW13, Q8
14	Analysis of sequential circuits	6.9	L6, HW14, Q9
15	FSM design examples	6.7, 6.8	HW15, Q10

Final Exam Information

The final Exam will be Tuesday May 6, 2016 in FPAT 263.

Mid-term Grade

Mid-term grades will be posted in myUK by the deadline established in the
Academic Calendar (http://www.uky.edu/registrar/content/academic-calendar)

Course Policies:

Submission of Assignments:

UK Canvas (uk.instructure.com) will be used to submit all graded material for credit in
this course. UK Canvas will also be used for posting class announcements and
assignments. Use your Link Blue login and password to access Canvas based courses.
Canvas is also accessible through a smartphone app. Students are responsible for
regularly checking the class Canvas site and checking email.

Attendance Policy:

Students are expected to withdraw from the class if more than 20% of the classes
scheduled for the semester are missed (excused or unexcused) per university policy.

Excused Absences

Students need to notify the professor of absences prior to class when possible. *Senate Rules
5.2.4.2* defines the following as acceptable reasons for excused absences: (a) serious illness,
(b) illness or death of family member, (c) University-related trips, (d) major religious
holidays, and (e) other circumstances found to fit "reasonable cause for nonattendance" by
the professor.

Students anticipating an absence for a major religious holiday are responsible for notifying
the instructor in writing of anticipated absences due to their observance of such holidays
no later than the last day in the semester to add a class. Two weeks prior to the absence is
reasonable, but should not be given any later. Information regarding major religious
holidays may be obtained through the Ombud (859-257-3737,
http://www.uky.edu/Ombud/ForStudents ExcusedAbsences.php.

Students are expected to withdraw from the class if more than 20% of the classes
scheduled for the semester are missed (excused) per University policy.

Per *Senate Rule 5.2.4.2*, students missing any graded work due to an excused absence are
responsible: for informing the Instructor of Record about their excused absence within one
week following the period of the excused absence (except where prior notification is
required); and for making up the missed work. The professor must give the student an
opportunity to make up the work and/or the exams missed due to an excused absence, and

shall do so, if feasible, during the semester in which the absence occurred.

Verification of Absences

Students may be asked to verify their absences in order for them to be considered excused. *Senate Rule 5.2.4.2* states that faculty have the right to request "appropriate verification" when students claim an excused absence because of illness, or death in the family. Appropriate notification of absences due to University-related trips is required prior to the absence when feasible and in no case more than one week after the absence.

Academic Integrity

Per University policy, students shall not plagiarize, cheat, or falsify or misuse academic records. Students are expected to adhere to University policy on cheating and plagiarism in all courses. The minimum penalty for a first offense is a zero on the assignment on which the offense occurred. If the offense is considered severe or the student has other academic offenses on their record, more serious penalties, up to suspension from the University may be imposed.

Plagiarism and cheating are serious breaches of academic conduct. Each student is advised to become familiar with the various forms of academic dishonesty as explained in the Code of Student Rights and Responsibilities. Complete information can be found at the following website: http://www.uky.edu/Ombud. A plea of ignorance is not acceptable as a defense against the charge of academic dishonesty. It is important that you review this information as all ideas borrowed from others need to be properly credited.

Senate Rules 6.3.1 (see http://www.uky.edu/Faculty/Senate/ for the current set of *Senate Rules*) states that all academic work, written or otherwise, submitted by students to their instructors or other academic supervisors, is expected to be the result of their own thought, research, or self-expression. In cases where students feel unsure about a question of plagiarism involving their work, they are obliged to consult their instructors on the matter before submission.

When students submit work purporting to be their own, but which in any way borrows ideas, organization, wording, or content from another source without appropriate acknowledgment of the fact, the students are guilty of plagiarism.

Plagiarism includes reproducing someone else's work (including, but not limited to a published article, a book, a website, computer code, or a paper from a friend) without clear attribution. Plagiarism also includes the practice of employing or allowing another person to alter or revise the work, which a student submits as his/her own, whoever that other person may be. Students may discuss assignments among themselves or with an instructor or tutor, but when the actual work is done, it must be done by the student, and the student alone.

When a student's assignment involves research in outside sources or information, the student must carefully acknowledge exactly what, where and how he/she has employed them. If the words of someone else are used, the student must put quotation marks around

the passage in question and add an appropriate indication of its origin. Making simple changes while leaving the organization, content, and phraseology intact is plagiaristic. However, nothing in these Rules shall apply to those ideas, which are so generally and freely circulated as to be a part of the public domain.

Please note: Any assignment you turn in may be submitted to an electronic database to check for plagiarism.

Accommodations due to disability

If you have a documented disability that requires academic accommodations, please see me as soon as possible during scheduled office hours. In order to receive accommodations in this course, you must provide me with a Letter of Accommodation from the Disability Resource Center (DRC). The DRC coordinates campus disability services available to students with disabilities. It is located on the corner of Rose Street and Huguelet Drive in the Multidisciplinary Science Building, Suite 407. You can reach them via phone at (859) 257-2754 and via email at drc@uky.edu. Their web address is http://www.uky.edu/StudentAffairs/DisabilityResourceCenter/.

New Course Form

Open in full window to print or save

Generate R

Attachments:

[Browse...]   Upload File

ID	Attachment
Delete 6016	EE282syllabusV5.docx

[First] 1 [Last]

(*denotes required fields)

1. **General Information**

   a. * Submitted by the College of: ENGINEERING   Submission Date: 9/29/2015

   b. * Department/Division: Electrical and Computer Engineering

   c.
   * Contact Person Name: James Lumpp   Email: jel@uky.edu   Phone: 7-3895
   * Responsible Faculty ID (if different from Contact)   Email: Phone:

   d. * Requested Effective Date: ⦿ Semester following approval OR ◯ Specific Term/Year [1]

   e.
   Should this course be a UK Core Course? ◯ Yes ⦿ No

   If YES, check the areas that apply:

   ☐ Inquiry - Arts & Creativity   ☐ Composition & Communications - II
   ☐ Inquiry - Humanities   ☐ Quantitative Foundations
   ☐ Inquiry - Nat/Math/Phys Sci   ☐ Statistical Inferential Reasoning
   ☐ Inquiry - Social Sciences   ☐ U.S. Citizenship, Community, Diversity
   ☐ Composition & Communications - I   ☐ Global Dynamics

2. **Designation and Description of Proposed Course.**

   a. * Will this course also be offered through Distance Learning? ◯ Yes [1] ⦿ No

   b. * Prefix and Number: EE 282

   c. * Full Title: Digital Logic Design

   d. Transcript Title (if full title is more than 40 characters):

   e. To be Cross-Listed [2] with (Prefix and Number): CpE 282

   f. * Courses must be described by at least one of the meeting patterns below. Include number of actual contact hours[3] for each meeting pattern type.

3	Lecture	3	Laboratory[1]		Recitation		Discussion
	Indep. Study		Clinical		Colloquium		Practicum
	Research		Residency		Seminar		Studio
	Other	If Other, Please explain:					

   g. * Identify a grading system:
   ⦿ Letter (A, B, C, etc.)
   ◯ Pass/Fail
   ◯ Medicine Numeric Grade (Non-medical students will receive a letter grade)
   ◯ Graduate School Grade Scale

   h. * Number of credits: 4

   i. * Is this course repeatable for additional credit? ◯ Yes ⦿ No
   If YES: Maximum number of credit hours:
   If YES: Will this course allow multiple registrations during the same semester? ◯ Yes ◯ No

j. * Course Description for Bulletin:

Boolean algebra; number systems; combinational logic circuits; synchronous sequential circuits; asynchronous sequential circuits; design problems using digital logic. Laboratory experiments reinforce the course content. Lecture, three hours; laboratory, one three-hour session.

k. Prerequisites, if any:

EGR 102 or equivalent programming course.

l. Supplementary teaching component, if any: ○ Community-Based Experience ○ Service Learning ○ Both

3. * Will this course be taught off campus? ○ Yes ⦿ No

If YES, enter the off campus address:

4. Frequency of Course Offering.

   a. * Course will be offered (check all that apply): ☑Fall ☑Spring ☐Summer ☐Winter

   b. * Will the course be offered every year? ⦿ Yes ○ No

      If No, explain:

5. * Are facilities and personnel necessary for the proposed new course available? ⦿ Yes ○ No

If No, explain:

6. * What enrollment (per section per semester) may reasonably be expected? 175

7. Anticipated Student Demand.

   a. * Will this course serve students primarily within the degree program? ⦿ Yes ○ No

   b. * Will it be of interest to a significant number of students outside the degree pgm? ⦿ Yes ○ No

      If YES, explain:

Required by BS Computer Engineering and BS Electrical Engineering degrees.

8. * Check the category most applicable to this course:

☑Traditional – Offered in Corresponding Departments at Universities Elsewhere
☐Relatively New – Now Being Widely Established
☐Not Yet Found in Many (or Any) Other Universities

9. Course Relationship to Program(s).

   a. * Is this course part of a proposed new program? ○ Yes ⦿ No

      If YES, name the proposed new program:

   b. * Will this course be a new requirement [5] for ANY program? ⦿ Yes ○ No

      If YES [5], list affected programs::

BS Computer Engineering and BS Electrical Engineering

10. Information to be Placed on Syllabus.

   a. * Is the course 400G or 500? ○ Yes ⦿ No

      If YES, the *differentiation for undergraduate and graduate students must be included* in the information required in 10.b. You must include: (i) identi additional assignments by the graduate students; and/or (ii) establishment of different grading criteria in the course for graduate students. (See SR

   b. ☑* The syllabus, including course description, student learning outcomes, and grading policies (and 400G-/500-level grading differentiation if appl

      10.a above) are attached.

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[1] Courses are typically made effective for the semester following approval. No course will be made effective until all approvals are received.
[2] The chair of the cross-listing department must sign off on the Signature Routing Log.

[1] In general, undergraduate courses are developed on the principle that one semester hour of credit represents one hour of classroom meeting per week for a semester, exclusive of any laboratory meeting. Laboratory meeting, generally, re two hours per week for a semester for one credit hour. (from SR 5.2.1)
[2] You must also submit the Distance Learning Form in order for the proposed course to be considered for DL delivery.
[3] In order to change a program, a program change form must also be submitted.

Rev 8/09